SHF-0289

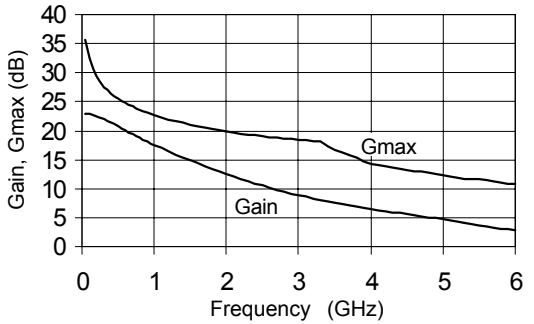
0.05 - 6 GHz, 1.0 Watt GaAs HFET

Product Description

Sirenza Microdevices' SHF-0289 is a high performance AlGaAs/GaAs Heterostructure FET (HFET) housed in a low-cost surface-mount plastic package. The HFET technology improves breakdown voltage while minimizing Schottky leakage current resulting in higher PAE and improved linearity.

Output power at 1dB compression for the SHF-0289 is +30dBm when biased for Class AB operation at 7V,200mA. The +43 dBm third order intercept makes it ideal for high dynamic range, high intercept point requirements. It is well suited for use in both analog and digital wireless communication infrastructure and subscriber equipment including 3G, cellular, PCS, fixed wireless, and pager systems.

Typical Gain Performance (7V,200mA)



Product Features

- **High Linearity Performance at 1.96 GHz**
  - **+30 dBm P1dB**
  - **+43 dBm OIP3**
  - **+23.7 dBm IS-95 Channel Power**
  - **+14.6 dB Gain**
- **+21.7 dBm W-CDMA Channel Power**
- **High Drain Efficiency (>50% at P1dB)**
- **See App Note AN-032 for circuit details**

Applications

- **Analog and Digital Wireless Systems**
- **3G, Cellular, PCS**
- **Fixed Wireless, Pager Systems**

Symbol	Device Characteristics	Test Conditions, 25C V_{DS}=7V, I_{DQ}=200mA (unless otherwise noted)	Test Frequency	Units	Min	Typ	Max
Gmax	Maximum Available Gain	$Z_S=Z_S^*$, $Z_L=Z_L^*$	0.90 GHz 1.96 GHz 2.14 GHz	dB dB dB	- - -	23 20 19.5	- - -
S_{21}	Insertion Gain [1]	$Z_S=Z_L$= 50 Ohms	0.90 GHz	dB	16.7	18.5	20.3
Gain	Power Gain [2]	Application Circuit	1.96 GHz	dBm	13.1	14.6	16.1
OIP3	Output Third Order Intercept Point [2]	Application Circuit	1.96 GHz	dBm	40.5	43.0	-
P1dB	Output 1dB Compression Point [2]	Application Circuit	1.96 GHz	dBm	28.7	30.2	-
P_{CHAN}	IS-95 Channel Power (-45dBc ACPR)	Application Circuit	1.96 GHz	dBm	-	23.7	-
NF	Noise Figure [2]	Application Circuit	1.96 GHz	dB	-	4.0	-
I_{DSS}	Saturated Drain Current	V_{DS}= V_{DSP}, V_{GS}= 0V		mA	408	588	768
g_m	Tranconductance	V_{DS}= V_{DSP}, V_{GS}= -0.25V		mS	288	396	504
V_P	Pinch-Off Voltage [1]	V_{DS}= 2.0V, I_{DS}= 1.2mA		V	-3.0	-1.9	-1.0
BV_{GS}	Gate-Source Breakdown Voltage [1]	I_{GS}= 2.4mA, drain open		V	-	-17	-15
BV_{GD}	Gate-Drain Breakdown Voltage [1]	I_{GD}= 2.4mA, V_{GS}= -5.0V		V	-	-22	-17
Rth	Thermal Resistance	junction-to-lead		°C/W	-	41	-
V_{DS}	Operating Voltage [3]	drain-source		V	-	-	8.0
I_{DQ}	Operating Current [3]	drain-source, quiescent		mA	-	-	280
P_{DISS}	Power Dissipation [3]			C	-	-	1.4

[1] 100% tested - Insertion gain tested using a 50 ohm contact board (no matching circuitry) during final production test.
[2] Sample tested - Samples pulled from each wafer/package lot. Sample test specifications are based on statistical data from sample test measurements. The test fixture is an engineering application circuit board. The application circuit was designed for the optimum combination of linearity, P1dB, and VSWR.
[3] Maximum recommended power dissipation is specified to maintain T_J<140C at T_L=85C. V_{DS} * I_{DQ}< 1.4W is recommended for continuous reliable operation.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	400	mA
Forward Gate Current	I_{GSF}	2.4	mA
Reverse Gate Current	I_{GSR}	2.4	mA
Drain-to-Source Voltage	V_{DS}	+9.0	V
Gate-to-Source Voltage	V_{GS}	<-5 or >0	V
RF Input Power	P_{IN}	400	mW
Operating Lead Temperature	T_L	See Graph	°C
Storage Temperature Range	T_{stor}	-40 to +165	°C
Power Dissipation	P_{DISS}	See Graph	W
Channel Temperature	T_J	+165	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

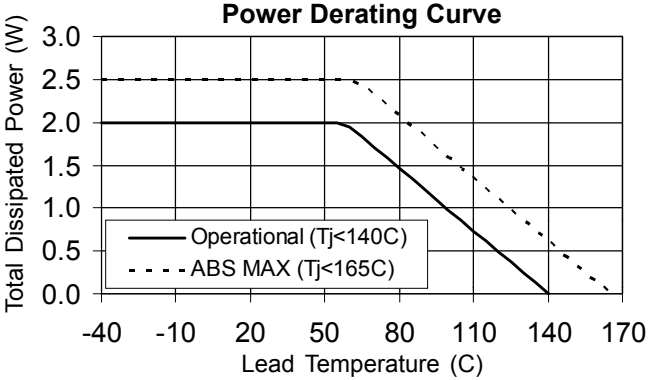
MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the bias condition should also satisfy the following expression:

$$P_{DC} < (T_J - T_L) / R_{TH}$$

where:

$P_{DC} = I_{DS} * V_{DS}$ (W)
T_J = Junction Temperature (°C)
T_L = Lead Temperature (pin 4) (°C)
R_{TH} = Thermal Resistance (°C/W)

Power Derating Curve



Design Considerations and Trade-offs

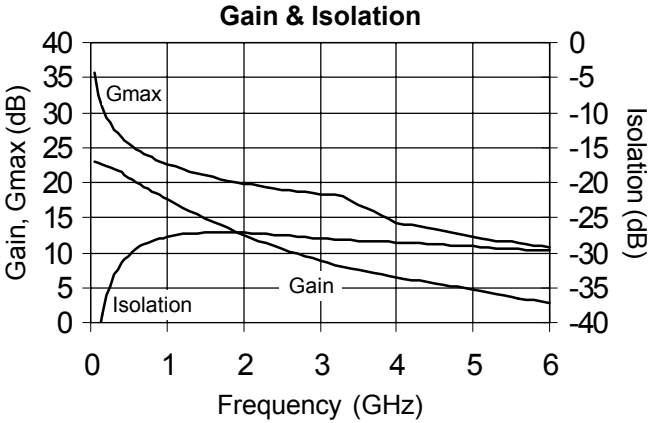
1. The SHF-0x89 is a depletion mode FET and requires a negative gate voltage. Normal pinchoff variation from part-to-part precludes the use of a fixed gate voltage for all devices. Active bias circuitry or manual gate bias alignment is recommended to maintain acceptable performance (RF and thermal).

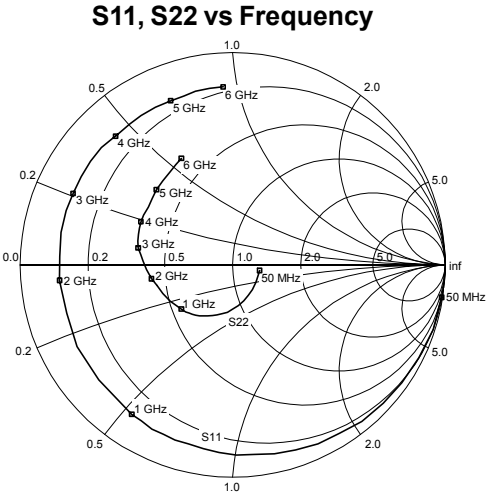
2. Active bias circuitry is strongly recommended for class A operation (backoff >6dB).

3. For large signal operation (< 6dB backoff) class AB operation is required to maximize the FET's performance. Passive gate bias circuitry is generally required to achieve pure class AB performance. This is generally accomplished using a voltage divider with temperature compensation. Per item 1 above the gate voltage should be aligned for each device to eliminate the effects of pinchoff process variation.

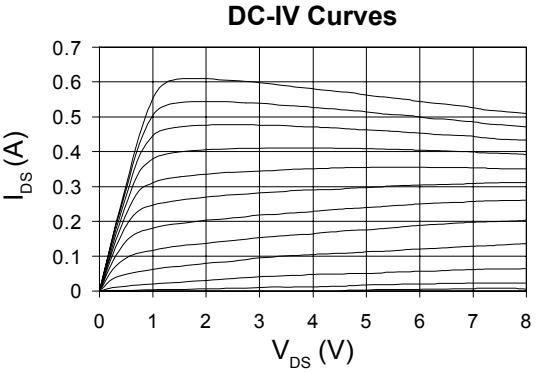
4. Choose the operating voltage based on the amount of backoff. For large signal operation the drain-source voltage should be increased to 8V to maximize P1dB. For small signal operation the OIP3 may be improved by reducing the voltage and increasing the current. The recommended application circuit should be re-optimized if the recommended 7V bias condition is not used. Make sure the quiescent bias condition does not exceed the recommended power dissipation limit (shown on page 1).

De-embedded S-Parameters (Z_S=Z_L=50 Ohms, V_{DS}=7V, I_{DS}=200mA, 25°C)





Note: S-parameters are de-embedded to the device leads with Z_S=Z_L=50Ω. The data represents typical performace of the device. De-embedded s-parameters can be downloaded from our website (www.sirenza.com).



V_{GS} = -2.0 to 0V, 0.2V steps
T=25°C

Typical Performance - Engineering Application Circuits (See App Note AN-032)

Freq (MHz)	V_{DS} (V)	I_{DQ} (mA)	P1dB (dBm)	-45dBc Channel Power (dBm)	-55dBc Channel Power (dBm)	OIP3[6] (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
900	7	200	30.2	23.5[4]	21.1[4]	43.0	19.2	-15	-12	3.2
1960	7	200	30.2	23.7[4]	21.3[4]	43.0	14.6	-18	-10	4.0
2140	7	200	30.3	21.7[5]	20.4[5]	43.0	13.8	-18	-7	4.1

[4] IS-95 CDMA Channel Power (9 Fwd Channels, 885kHz offset, 30kHz Adj Chan BW)
[5] W-CDMA Channel Power (64 DPCH, 5MHz offset, 3.84MHz Adj Chan BW)
[6] P_{OUT}= +13dBm per tone, 1MHz tone spacing

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Pin Description

Pin #	Function	Description
1	Gate	RF Input
2	Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output
4	Source	Same as Pin 2

Mounting and Thermal Considerations

It is very important that adequate heat sinking be provided to minimize the device junction temperature. The following items should be implemented to maximize MTTF and RF performance.

1. Multiple solder-filled vias are required directly below the ground tab (pin 4). [CRITICAL]
2. Incorporate a large ground pad area with multiple plated-through vias around pin 4 of the device. [CRITICAL]
3. Use two point board seating to lower the thermal resistance between the PCB and mounting plate. Place machine screws as close to the ground tab (pin 4) as possible. [CRITICAL]
4. Use 2 ounce copper to improve the PCB's heat spreading capability. [RECOMMENDED]

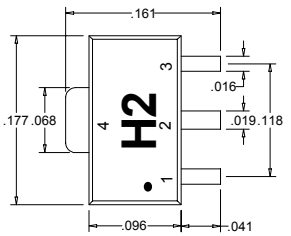
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SHF-0289	7"	1000

Part Symbolization

The part will be symbolized with the "H2" designator and a dot signifying pin 1 on the top surface of the package.

Package Dimensions



DIMENSIONS ARE IN INCHES

Recommended Mounting Configuration for Optimum RF and Thermal Performance